

**REMARKS**

Claims 1, 2, 8-10, 12, 13, 18, 19, 21 and 27 have been amended and Claims 11, 17, 24-26 and 28 have been canceled. Claims 1-10, 12-16, 18-23 and 27 remain pending in this application.

**I. Rejection of Claims 1 and 24 under Section 102**

Claims 1 and 24 stand rejected under Section 102(e) as being anticipated by Laor et al.

The office action states that Laor et al. teaches a phase locked loop (PLL) that receives a word clock (WC) signal and generates a first clock that is a multiple of the WC signal. It is also stated that Laor teaches a clock generator that receives the first clock signal and generates a plurality of second clock signals that are submultiples of the first clock signal.

Laor et al teaches a synchronous pipelined switch using a serial transmission. Specifically, Laor is used for converting input from serial to parallel for synchronous output for the purposes of operating a switch. The switch includes a PLL for each interface which synchronizes to the serial input from that input interface. Also, output interfaces each include a PLL which synchronizes to the serial output from the switch interconnect. Laor's system includes a single frequency source which is analogous to the input word clock (WC) of the present invention. In Laor, the WC is inputted in multiple interface cards which each have their own PLL (see references 205, 241 in Figs. 1 and 2). Each of the PLLs in the multiple interface cards can receive the WC and create a "first clock" based on the WC. A second PLL is required to create the "second clock signals" which are submultiples of the first clock signal.

Turning the example cited in the office action, the WC is considered clock A which is inputted into the first PLL 205 to generate the first clock signal 206. Via shift register 202, the first clock signal 206 is then inputted into a second PLL 211 which, in turn

generates multiple clocks, namely clock B and clock B/10. Thus, Laor requires the use of multiple PLLs to carry out the invention and successfully generate multiple clocks.

In similar fashion to Laor, Applicant's invention employed a word clock that is used to create multiple clocks for later use. However, the data system of the present has a completely different fundamental structure compared to the construction of Laor. More specifically, the system of the present invention provides a minimal interface for serial data transmission. As stated in the specification, there is a desire to reduce the overall size and complexity of the data transmission interface. See page 2, lines 1-7. Conventional transmitters and receivers are not integrated onto a single chip due to the size of the phase locked loop (PLL) typically included in the devices. A typical PLL is composed of a resistor and capacitor where the size of the combination of these elements is too large for a single chip. Using more than one chip for the transmitter or receiver increases the cost and size of the system. There has been a desire in the industry to have a receiver and transmitter that are small and both integrated on a single chip.

Unlike Laor, the system of the present invention uses only a single PLL in its design, such as in a transmitter. As seen in Fig. 3, for example, a word clock WC is received by a single PLL that creates a first clock, which can be a system clock. That system clock is then received by a small clock generator, not by another PLL as what is carried out in Laor. The clock generator, rather than another large PLL, is what is employed in the present invention to generate a plurality of second clock signals that have frequencies that are submultiples of the first clock. As a result, the system of the present invention can be kept on a small scale to permit incorporate into a single chip, as set forth in the present application. This carries out the goal of the present invention which is to provide a serial data transmission system with a minimal interface.

Laor, in contrast, has many, many interfaces. This runs contrary to the intent, as set forth in the present claims, of Applicant's invention. Each of these required multiple interfaces each include their own separate PLL. See Figs. 1 and 2. This large scale, multiple interface system design allows Laor the luxury of using multiple PLL. This is not surprising because Laor is being used in a switching environment where system space is not a concern.

Claim 1 has been amended to reflect that a single PLL is employed in given device, such as transmitter, whereby that PLL generates a first clock. In the present invention, a clock generator (not a PLL as in Laor) receives the first clock to generate multiple clocks for use by a circuit designer. The unique system design of the present invention completely obviates the need for a second large PLL for generating multiple clocks. Thus, the system of the present invention is more compact than prior art interfaces. Moreover, the unique design of Applicant's PLL, as in amended Claim 27, further facilitates the ability to incorporate the entire system on a single chip.

In view of the foregoing, Applicant submits that Laor fails to anticipate Claim 1, as amended. Claim 1 is now allowable over the cited prior art.

Laor has also been cited against Claim 24. The rejection of Claim 24 is moot in light of the cancellation thereof.

## II. Rejection of Claim 27 under Section 102

Claim 27 stands rejected under Section 102(b) as being anticipated by Campbell. The limitations of allowed Claim 28 have been incorporated into base Claim 27. Therefore, Claim 27 is now allowable over the cited prior art.

## III. Rejection of Claims 2-9 under Section 103

Claims 2-9 stand rejected under Section 103(a) as being unpatentable over Laor in view of Fujita.

### Claim 2

As to Claim 2, the office action states that Laor teaches a clock generator that outputs one of the second clock signals having a same frequency as the WC signal. The office action also states that Laor does not use a received second clock to adjust the first clock. Fujita is cited for the teaching of a feedback circuit to adjust the first clock (system clock). Fujita specifically teaches the feedback of multiple frequency divided clocks back into the PLL oscillation circuit. However, in the present invention, Claim 2 requires that only one of the multiple clocks is fed back into the PLL. Therefore, Fujita fails to disclose the feedback construction as required by Claim 2.

Further, Claim 2 depends from now allowable Claim 1. Therefore, Claim 2 is also submitted as being allowable.

Claim 3

Claim 3 depends from now allowable Claim 1. Therefore, Claim 3 is also submitted as being allowable.

Claim 4

Claim 4 depends indirectly from now allowable Claim 1. Therefore, Claim 4 is also submitted as being allowable.

Claim 5

Claim 5 depends indirectly from now allowable Claim 1. Therefore, Claim 5 is also submitted as being allowable.

Claim 6

Claim 6 depends indirectly from now allowable Claim 1. Therefore, Claim 6 is also submitted as being allowable.

Claim 7

Claim 7 depends indirectly from now allowable Claim 1. Therefore, Claim 7 is also submitted as being allowable.

Claim 8

Claim 8 depends from now allowable Claim 1. Therefore, Claim 8 is also submitted as being allowable.

Claim 9

Claim 9 depends indirectly from now allowable Claim 1. Therefore, Claim 9 is also submitted as being allowable.

**IV. Rejection of Claims 10-23, 25 and 26 under Section 103**

Claims 10-23, 25 and 26 as being unpatentable over Bowers in view of Laor et al. The office action states that Bowers discloses a serial communication system with a clock generator for affecting serial data transmission and control between a master chip and the devices. The master chip is considered to be the transmitter while an IC device is considered to be a receiver. It is presented that Bowers teaches a transmitter for receiving the WC signal and a receiver for receiving the WC signal. The office action states that Bowers does not provide for generating a plurality of clock signals based on the word clock.

Claim 10

Laor is cited for the teaching of receiving a word clock signal and a second means for generating a plurality of clock signals based on the WC. In the broadest sense, Laor does, in fact, have a means to generate a plurality of clock signals that are generally based on the WC signal. However, the structure to carry this out is completely different compared to the system of the present invention. As stated above in connection with Section I, above, Laor requires multiple PLLs, one for creating the first clock and another PLL for creating each additional clock.

The system of the present invention does not use multiple PLLs for each device (e.g. transmitter or receiver). The means for generating multiple clocks in the present invention is a single PLL and a clock generator. The means for generating multiple

clocks, as stated above, is two or more PLLs. The use of multiple large PLLs in Laor's system makes it large and difficult to incorporate into a single chip.

Claim 10 includes limitations for both sides of the system, namely, the transmitter and the receiver. Thus, one PLL and one clock generator is used on each device. Laor requires a total of four PLLs, two for each device.

Therefore, Bowers and Laor fail to teach the present invention, as Claim 10, as amended. Claim 10 is now allowable over the cited prior art.

#### Claims 11-23

Claims 11-23 depend directly or indirectly from base Claim 10. Since Claim 10 is now allowable over the cited prior art, Applicant submits that Claims 11-23 are now also allowable.

#### Claims 25 and 26

The rejection of Claims 25 and 26 is moot in light of the cancellation of these claims.

#### **V. Allowable Subject Matter**

The office action states that Claim 28 is objected to but would be allowed if all of its limitations are incorporated into the base claim. Accordingly, Applicant has incorporated all of the limitations of allowed Claim 28 into base Claim 27. As a result, Claim 27 is now allowable over the cited prior art.

#### **VI. Conclusion**

Applicant submits that claims, as amended, are allowable over the cited prior art. In view of the above, Applicants submit that pending Claims are now in condition for allowance. Reconsideration of the Rejections and Objections are requested. Allowance of Claims 1-10, 12-16, 18-23 and 27 at an early date is solicited.

If an extension of time is required for timely submission of this response, Applicant hereby petitions for an appropriate extension of time and the Office is

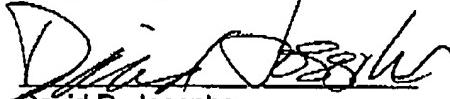
authorized to charge Deposit Account 02-0900 for the appropriate additional fees in connection with the filing of this response.

The Examiner is invited to telephone the undersigned should any questions arise.

Respectfully submitted,

Dated:

March 16, 2004



David R. Josephs

Registration No. 34,632

BARLOW, JOSEPHS & HOLMES, LTD.

101 Dyer Street, 5<sup>th</sup> Floor

Providence, RI 02903

Tel: 401-273-4446

Fax: 401-273-4447